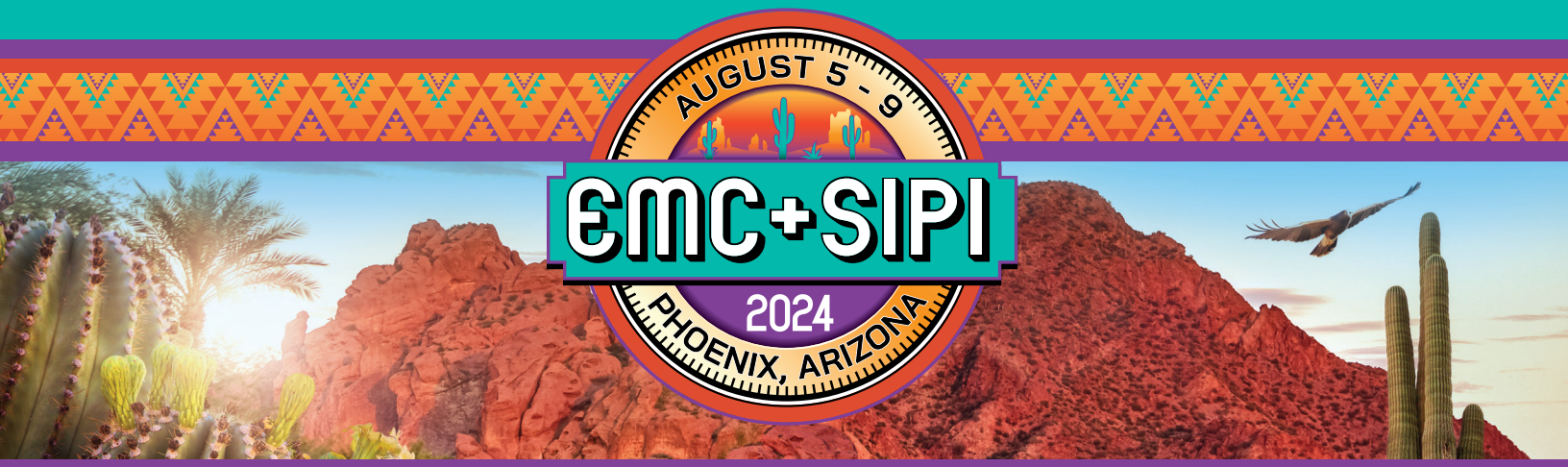
2024 IEEE INTERNATIONAL SYMPOSIUM ON ELECTROMAGNETIC COMPATIBILTY, SIGNAL & POWER INTEGRITY



ANNOUNCING THE INAUGURAL COURSE

Global Signal Integrity and Power Integrity (SIPI) University

WEDNESDAY, AUGUST 7, 2024

COURSE OVERVIEW: Signal integrity (SI) and power integrity (PI) are gaining an ever-growing attention due to today's higher data rates and larger currents in high-speed digital systems. Industries call for skilled engineers with both basic and advanced background in these two disciplines. Courses dealing with SI and PI related topics at academic level are limited and offered by only a few institutions and research laboratories in the US and worldwide. The inaugural **"Global SIPI University"** aims at bridging this gap with a one-day introductory course at the Electromagnetic and Signal & Power Integrity Symposium to be held in Phoenix, Arizona, from August 5-9, 2024.

The mission of the **"Global SIPI University"** is to provide technicians and engineers the opportunity to acquire SI and PI concepts from experienced and well-known instructors from both industry and academia. The **"Global SIPI University"** offers a rigorous background directly linked with practical problems and solutions. Attendees will acquire application-oriented skills and knowledge about the need for signal and power integrity analysis as well as the tools and methods available for tackling SI and PI related problems. Basic and fundamental concepts involving limited but relevant theory will be offered to fully understand how practical problems can be approached using analytical methods, simulation tools, as well as measurements to validate simulations. Instructors will discuss design examples to provide a clear insight and processes for guiding the attendee towards problem solutions.

Please see the symposium website using the QR Code provided to view the registration fees, presentation abstracts, and instructor biographies. Note the course size is LIMITED to ensure interaction between the attendees and the instructors. Seats will be available on a first-come, first-served basis.

www.emc2024.org

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TIME	TOPIC	PRESENTER/INSTRUCTOR
08:00 – 8:30	**Registration / Introductions**	**Christian Schuster** and **Francesco de Paulis**
08:30 – 09:15	**Opening:** Progression of SIPI Modeling: A 50-Year Journey to Modern System Design Challenges	**Dr. Albert Ruehli** *(Missouri University of Science and Technology)* **Mr. Stephen Scearce** *(Cisco Systems)*
09:15 – 10:00	**Keynote:** Global industry trends and demands from a system and packaging perspective	**Dr. Kemal Aygün** *(Intel)*
10:00 – 10:30	**Coffee Break / Networking**	
10:30 – 11:15	**Signal Integrity I:** Passive interconnect design, lumped effects, transmission line effects	**Dr. Bhyrav Mutnury** *(AMD)*
11:15 – 12:00	**Signal Integrity II:** Electrical Signaling — Modulation, Equalization, and Channel Design	**Dr. Wendem Beyene** *(Meta)*
12:00 – 13:30	**Lunch Break / Networking**	
13:30 – 14:15	**Signal Integrity III:** Signal integrity measurements and simulation	**Dr. Eric Bogatin** *(University of Colorado, Boulder)*
14:15 – 15:00	**Power Integrity I:** Fundamentals of power integrity with practical analysis techniques for current and emerging designs	**Dr. Ihsan Erdin** *(Celestica)*
15:00 – 15:30	**Coffee Break / Networking**	
15:30 – 16:15	**Power Integrity II:** VRM, package/IC-level PDN design	**Dr. Chulsoon Hwang** *(Missouri University of Science and Technology)*
16:15 – 17:30	**The Future of SI & PI Engineering:** Open discussion with all instructors and attendees	**Christian Schuster** and **Francesco de Paulis**

CHAIR:
Christian Schuster
Hamburg University of Technology, Germany

Christian Schuster (IEEE Senior Member) received a Diploma degree in Physics in 1996 and a Ph.D. degree in electrical engineering in 2000. Since 2006, he is a Full Professor at Hamburg University of Technology (TUHH), Germany. Prior to TUHH he was with the IBM T. J. Watson Research Center, Yorktown Heights, NY. His current interests include signal and power integrity of digital systems, multiport measurement and calibration techniques, and development of electromagnetic simulation methods for communication electronics. He serves as an Associate Editor for the IEEE Transactions on EMC as well as an Adjunct Associate Professor at the School of Electrical and Computer Engineering of the Georgia Institute of Technology.

CO-CHAIR:
Francesco de Paulis
University of L'Aquila, L'Aquila, Italy

Francesco de Paulis (Senior Member IEEE) received the M.S. degree in Electrical Engineering in May 2008 from Missouri University of Science and Technology (formerly University of Missouri-Rolla), USA, and the Ph.D. degree in Electrical and Information Engineering in 2012 from the University of L'Aquila, L'Aquila, Italy. He is currently an Associate Professor at the Electromagnetic Compatibility and Signal Integrity Laboratory at the University of L'Aquila. His main research interests are in signal and power integrity, high speed channel design and optimization, composite materials for shielding and absorption, RF interference in mixed-signal system, TSVs in silicon chips and interposers, antenna design and measurement techniques, remote fault detection in transmission lines, microwave design of electronic devices and systems for space applications.

COURSE SYLLABUS

EMC+SIPI 2024 — AUGUST 5 - 9 — PHOENIX, ARIZONA

Title: Progression of SIPI Modeling: A 50-Year Journey to Modern System Design Challenges

Opening: Albert Ruehli and Stephen Scearce

Abstract: The introductory combined presentations cover the evolution of SIPI including today's challenges. The first part presents the evolution of the SIPI approach from its start 50 years ago. SIPI was originally driven by large high speed mainframe computer designs such as IBM's. With time, the increase in performance of IC's made the SIPI modeling a general necessity which resulted in new companies providing SIPI design tools. The increase in system performance brought about significant improvement of high performance in solvers with other advantages such as graphical user interfaces. In this presentation, we also describe the challenges in modern system for High-Speed Serdes design and the latest DDR5 implementations. Other issues are considered such as the large current and power delivery challenges in high performance systems.

Title: Global Industry Trends & Demands - Systems and Packaging Perspective

Keynote: Kemal Aygün

Abstract: With the emergence of new applications such as artificial intelligence, electronic systems need to provide increasingly improved performance. One area where the performance demand has been scaling very aggressively is for interconnecting different components in a system with high-speed/high-bandwidth signaling. This presentation will review some of the recent global trends and demands in this area, from both a systems and a packaging perspective. Emergence and evolution of 'system-in-package' architectures, corresponding interconnect technologies, and some key SI/PI challenges will be described. Finally, some recent advances on standardization of on-package high-speed signaling interconnects, that complement existing system-level standards will also be discussed.

Title: High-Speed Signal Integrity Challenges for Next Generation

Signal Integrity I: Bhyrav Mutnury

Abstract: The challenges associated with high-speed signal integrity (SI) are becoming exponentially complex with the doubling of signal speeds every generation. In this presentation, high-speed server design is used an example to demonstrate the next generation SI challenges and potential opportunities to overcome these challenges. The presentation covers basics of SI, high-speed interconnects, analog and digital equalization and high-speed challenges beyond 32 Gbps. The presentation also touches up some AI/ML use cases for next generation challenges.

Title: Electrical Signaling — Modulation, Equalization, and Channel Design

Signal Integrity II: Wendem Beyene

Abstract: The presentation explores different modulation and signaling techniques with the goal to achieve over 224-Gb/s link speed through electrical signaling. The focus of this work spans from interconnects to transceiver architecture from system, channel and signaling point of view. In addition to traditional multilevel signaling pulse amplitude modulations (PAM-4, PAM-8, ⋯). This talk also compares simultaneous bidirectional signaling and multiwire encoding techniques as potential solutions for even higher data rates. These signaling options are compared both from a performance and implementation complexity point of view with possible improvements required to further extend the speed and reach of electrical signaling.

Title: Signal Integrity Measurements and Simulation

Signal Integrity III: Eric Bogatin

Abstract: Measurement and simulation go hand in hand in any efficient design workflow. Simulation is used in both the pre-layout phase to establish accurate design rules and in the post-layout design phase to establish confidence in a design before committing large resources to the hardware. Measurements are critical to validate simulation processes and device or component models and characterize materials used as input to the simulation. This course will provide an introduction to some of the measurement and simulation tools available for SI/PI and EMI applications.

Title: Fundamentals of Power Integrity with Practical Analysis Techniques for Current and Emerging Designs

Power Integrity I: Ihsan Erdin

Abstract: Fundamental issues of PI will be laid out from a perspective with its direct relation to SI. The role of ground vias in multilayered boards will be explained in some practical PCB stackups. Basic decoupling concepts will be covered with placement and selection of bypass capacitors including the effects of interplane capacitance. Insights will be provided to inner workings of simulation methods for their efficient use in PI analysis and optimization. Practical PCB decoupling methodologies will be presented and challenges will be discussed for the emerging 100+ Gb/s designs including substrate decoupling of co-packaged optics and embedded discretes.

Title: VRM, Package/IC-level PDN Design

Power Integrity II: Chulsoon Hwang

Abstract: Continuing from PI I, the basic elements of a PDN, including on/off-chip VRM and package/IC-level PDN, along with their roles in power integrity, will be presented using practical examples. Additionally, challenges and research trends in recent PDN design will be introduced.

Title: The Future of SI & PI Engineering – Open discussion with all instructors and attendees.

Closing Session: Moderators Christian Schuster and Francesco de Paulis